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10/645,890	08/20/2003	Hee-Choul Lee	4234-13	8184

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EXAMINER	
SONI, KETAN S	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/645,890	LEE, HEE-CHOUL	
	Examiner	Art Unit	
	Ketan Soni	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/20/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/20/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *None*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement submitted on 08/20/2003 has been considered by the Examiner and made of record in the application file.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

1. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "broken" in claim 1-24 is used by the claim to mean "disconnected", while the accepted meaning is "unused." The term is indefinite because the specification does not clearly redefine the term.

2. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine

the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "breaking" in claim 1-24 is used by the claim to mean "destroying", or "disconnecting", while the accepted meaning is "rearranging" or "unused." The term is indefinite because the specification does not clearly redefine the term.

3. Claims 1-24 are vague and indefinite because claim: 1, line: 8-9, the term "the other coordinate" is unclear in the sense that which coordinate is described. Hence claims: 1-24 are vague and indefinite.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:
1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the Examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the Examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 - 21, and 23 - 26 are rejected under 35 U.S.C. 103 (a) as being unpatentable over **Thorson (US 5533198)** in view of **Passint et al. (US 6230252 B1).**

Consider **Claim:** 1, Thorson discloses, an n-dimensional broken mesh network (Fig: 1, and col: 4, lines: 59) comprising:

broken links which is generated by breaking connections between a starting switching element of each dimension and an ending switching element of each dimension (In n dimension field, relative co-ordinate defines movement from start to destination node, and a sign bit is attached, col: 6, lines: 16-20; additionally if the link between nodes rendered inoperable, communication is still possible by changing the direction, col: 5, lines: 55-58);

input output protocol processing blocks connected to the broken links (In order to transfer a packet info from a source node to a destination node within the network, routing information is formed and transformed, col: 8, lines: 4-7; additionally fig: 5 @ 52 processor; and Each look-up table entry 62 includes dimension locations 66.1-66.3 and sign bits 68.1-68.3 for each of the n possible dimensions. (As was explained earlier,

the sign bits indicate whether movement is to be in the PLUS or MINUS direction in a dimension), col: 10, lines: 44-48);

external traffic links connected to the input output protocol processing blocks (Processing Element, Fig: 5, Node 42 consists of a processing element 52 connected to a PLUS pathway 54 and a MINUS pathway 56, and Processing element 52 comprises one or more processors connected to one or more node memories, col: 8, lines: 34-37). Even though, Thorson discloses coordinates (fig: 4, 42.18, 42.19), processing elements, and switching elements, is generally silent about having n-1 same coordinates and the other coordinate is different only plus minus one,+-.1, when the coordinates are numbered monotone increasing way by increment 1.

However in the same field of endeavor, Passint et al. discloses and there are connections between two switching elements having n-1 same coordinates and the other coordinate is different only plus minus one,+-.1, when the coordinates are numbered monotone increasing way by increment 1 (Therefore, as illustrated in FIG. 3, this implementation of network transmits packets of information between the processor nodes in the + and - directions of three dimensions and routes packets to two nodes which both include four processors. In other words, one router chip 50 communicates directly with eight processors (130, 131, 132, 133, 130', 131', 132', and 133'), col: 6, lines: 65-68; additionally Fig: 19A, router table look up mechanism, 222 next incremented global addresses).

Therefore it would have been obvious to a person with ordinary skill in the art at the time the invention was made to incorporate and establishing a method for routing a

packet between a source and a destination node in a network system with n-dimensional topology as disclosed by Thorson with the method of Passint for increased fault tolerance.

Consider **Claim:** 2, and as applied to Claim: 1 above, Thorson as modified by Passint discloses the method according to claim 1. Further taught by combination and specifically by Thorson, that the system control processors connected to the broken links (Processing Element, Fig: 5, Node 42 consists of a processing element 52 connected to a PLUS pathway 54 and a MINUS pathway 56, and Processing element 52 comprises one or more processors connected to one or more node memories, col: 8, lines: 34-37).

Consider **Claim:** 3, and as applied to Claim: 2 above, Thorson as modified by Passint discloses the method according to claim 2. Further taught by combination and specifically by Passint, that the n-dimensional broken mesh network of claim 2, further comprising jumping routes which increase a number of input and output terminals in the switching element, wherein the jumping routes provides a connection between a switching element and other element having n-1 same coordinates and the other coordinate is different only plus minus one, .+-.1, when the coordinates are numbered monotone increasing way by increment 1, wherein other element comprises a switching element, input output protocol processor (Fig: 2, Processor 30, 32 and 30' , 32'), or system control processor (Fig: 2, Processor A).

Consider **Claim:** 4, and as applied to Claim: 2 above, Thorson as modified by Passint discloses the method according to claim 2. Further taught by combination and

specifically by Passint, where in the system control processors are connected by a control system bus (Fig: 1, processors 30 and 32 are connected by a bus).

Consider **Claim:** 5, and as applied to Claim: 4 above, Thorson as modified by Passint discloses the method according to claim 4. Further taught by combination and specifically by Passint where in n-dimensional broken mesh network (col: 3, lines: 23) of claim 4, further comprising jumping routes which increase a number of input and output terminals in the switching element (Fig: 3, routes: 152, 154, 156), wherein the jumping routes provides a connection between a switching element and other element having n-1 same coordinates and the other coordinate is different only plus minus one, .+-.1 (Fig: 3, + and - dimension), when the coordinates are numbered monotone increasing way by increment 1, wherein other element comprises a switching element, input output protocol processor, or system control processor (Fig: 3, processors, 130-133).

Consider **Claim:** 6, and as applied to Claim: 1 above, Thorson as modified by Passint discloses the method according to claim 1. Further taught by combination and specifically by Passint where in n-dimensional broken mesh network (col: 3, lines: 23) of claim 1, further comprising jumping routes which increase a number of input and output terminals in the switching element (Fig: 3, routes: 152, 154, 156), wherein the jumping routes provides a connection between a switching element and other element having n-1 same coordinates and the other coordinate is different only plus minus one, .+-.1 (Fig: 3, + and - dimension), when the coordinates are numbered monotone increasing way by increment 1, wherein other element comprises a switching element,

input output protocol processor, or system control processor (Fig: 3, processors, 130-133).

Consider **Claim:** 7, and as applied to Claim: 6 above, Thorson as modified by Passint discloses the method according to claim 6. Further taught by combination and specifically by Thorson where in the n-dimensional broken mesh network of claim 6, wherein internal switching elements are removed and adjacent elements are connected, or surface switching elements are removed and the input output protocol processors are connected to the link which is connected to the removed surface switching elements (In n dimension field, relative co-ordinate defines movement from start to destination node, and a sign bit is attached, col: 6, lines: 16-20; additionally if the link between nodes rendered inoperable, communication is still possible by changing the direction, col: 5, lines: 55-58).

Consider **Claim:** 8, and as applied to Claim: 7 above, Thorson as modified by Passint discloses the method according to claim 7. Further taught by combination and specifically by Passint, wherein connection between two switching elements having n-1 same coordinates and the other coordinate is different only plus minus one, .+-.1 (as illustrated in FIG. 3, this implementation of network transmits packets of information between the processor nodes in the + and - directions of three dimensions and routes packets to two nodes which both include four processors. In other words, one router chip 50 communicates directly with eight processors (130, 131, 132, 133, 130', 131', 132', and 133'), col: 6, lines: 65-68).

Consider **Claim:** 9, and as applied to Claim: 7 above, Thorson as modified by Passint discloses the method according to claim 7. Further taught by combination and specifically by Thorson, the n-dimensional broken mesh network of claim 7, wherein the input output protocol processor is connected to at least one of the switching element through the broken link or jumping route (In order to transfer a packet info from a source node to a destination node within the network, routing information is formed and transformed, col: 8, lines: 4-7; additionally fig: 5 @ 52 processor).

Consider **Claim:** 10, and as applied to Claim: 7 above, Thorson as modified by Passint discloses the method according to claim 7. Further taught by combination and specifically by Passint, the n-dimensional broken mesh network of claim 7, wherein the system control processor is connected to at least one of the switching element through the broken link or jumping route (Fig: 1, processors 30 and 32 are connected by a bus).

Consider **Claim:** 11, and as applied to Claim: 8 above, Thorson as modified by Passint discloses the method according to claim 8. Further taught by combination and specifically by Thorson, wherein the input output protocol processor is connected to at least one of the switching element through the broken link or jumping route (In order to transfer a packet info from a source node to a destination node within the network, routing information is formed and transformed, col: 8, lines: 4-7; additionally fig: 5 @ 52 processor; and Each look-up table entry 62 includes dimension locations 66.1-66.3 and sign bits 68.1-68.3 for each of the n possible dimensions. (As was explained earlier, the sign bits indicate whether movement is to be in the PLUS or MINUS direction in a dimension), col: 10, lines: 44-48).

Consider **Claim:** 12, and as applied to Claim: 8 above, Thorson as modified by Passint discloses the method according to claim 8. Further taught by combination and specifically by Thorson, wherein the system control processor is connected to at least one of the switching element through the broken link or jumping route (In order to transfer a packet info from a source node to a destination node within the network, routing information is formed and transformed, col: 8, lines: 4-7; additionally fig: 5 @ 52 processor; and Each look-up table entry 62 includes dimension locations 66.1-66.3 and sign bits 68.1-68.3 for each of the n possible dimensions. (As was explained earlier, the sign bits indicate whether movement is to be in the PLUS or MINUS direction in a dimension), col: 10, lines: 44-48).

Consider **Claim:** 13, and as applied to Claim: 5 above, Thorson as modified by Passint discloses the method according to claim 5. Further taught by combination and specifically by Passint, wherein each switching element comprises a switching controller, wherein the switching controller processes a control packet when the control packet is entered into the input buffer (when a message enters a router port, the message is inputted into the virtual channel buffer indicated by a virtual channel field in the sideband, col: 16, lines: 41-43). In addition Thorson discloses an input buffer with an input buffer monitor, and an output buffer (Each node processor will typically have its own memory and also can access some shared node memory, col: 4, lines: 62-63; and fig: 5 processing element 52 selects the path traveled by a message packet by accessing a look-up table stored in node memory, col: 8, lines: 55-57).

Consider **Claim:** 14, and as applied to Claim: 13 above, Thorson as modified by Passint discloses the method according to claim 13. Further taught by combination and specifically by Thorson, wherein each output buffer has an output buffer monitor, wherein when the output buffer is overloaded, the output buffer monitor reports to the switching controller to insert reporting data which is destined to the system control process into the output buffer or other output buffer (when a message enters a router port, the message is entered into the virtual channel buffer, and then indicated by a virtual channel field in the sideband for congestion relief, col: 16, lines: 41-43).

Consider **Claim:** 15, and as applied to Claim: 13 above, Thorson as modified by Passint discloses the method according to claim 13. Further taught by combination and specifically by Thorson, wherein the result of the processing the control packed by the switching controller is stored into arbitrary output buffer (If, for instance, node 42.18 wants to send a message to node 42.17, it would access the look-up table for the stored (buffered) entry stored for corresponding to node 42.17, col: 9, lines: 22-25 and col: 10, lines: 44-46).

Consider **Claim:** 16, and as applied to Claim: 13 above, Thorson as modified by Passint discloses the method according to claim 13. Further taught by combination and specifically by Thorson, wherein each switching element carries out dynamic self-routing (Direction ordering can be varied dynamically to enhance the fault tolerance of the system, as different routes can now have different corners, col: 5, lines: 48-50, and flexible routing col: 6, lines: 3-14). In addition Passint discloses dynamic self routing

(Global routing and local routing together provide routing information dynamically as they pass through network, col: 11, lines: 15-18).

Consider **Claim:** 17, and as applied to Claim: 16 above, Thorson as modified by Passint discloses the method according to claim 16. Further taught by combination and specifically by Passint, wherein if there is a packet to be delivered to a full output buffer, the packed is discarded when the packed is entered or the packed is in the front of the input buffer for routing (A router receives block 102, accepts data includes virtual channel management for keeping or discarding data, col: 11, lines: 10-13).

Consider **Claim:** 18, and as applied to Claim: 16 above, Thorson as modified by Passint discloses the method according to claim 16. Further taught by combination and specifically by Passint, wherein the packet in the front line of the input buffer (FIFO) is discarded, if there is no available output buffer for the next packet destination with available packet buffer space (A router receives block 102, accepts data includes virtual channel management, dynamically allocating memory queues similar to first in first out for keeping or discarding data, col: 11, lines: 10-13).

Consider **Claim:** 19, and as applied to Claim: 13 above, Thorson as modified by Passint discloses the method according to claim 13. Further taught by combination and specifically by Thorson, wherein the switching element stores the distance delta value of each jumping route to the switching element connected though the jumping route in the n-tuple delta values as (.DELTA.1, .DELTA.2, . . . , .DELTA.n), in list form of (axis direction, delta value), or in the list form of delta value for the fixed axis's in the system (If the link between nodes 12.14 and 12.11 is rendered inoperable, communication is

still possible simply by changing the direction ordering so as to change the occurrence of the -y move. In that case, the direction order routing method could be chosen as (+x, -y, z, -x, +y, -z) and the packet to be transferred between node 12.7 and node 12.11 will be transferred from node 12.7 to node 12.8 and then through nodes 12.5 and 12.2 to node 12.11, col: 5, lines: 63-67).

Consider **Claim:** 20, and as applied to Claim: 13 above, Thorson as modified by Passint discloses the method according to claim 13. Further taught by combination and specifically by Thorson, wherein the input protocol processor, system control processor, or the switching elements has the information (Fig: 5 @ 52 comprises one or more processors connected to buffer memories, col: 8, lines: 36-38) of the jumping routes in the form of n-tuple delta value as (.DELTA.1, .DELTA.2, . . . , .DELTA.n), in list form of (axis direction, delta value), or in the list form of delta value for the fixed axis's in the system (If the link between nodes 12.14 and 12.11 is rendered inoperable, communication is still possible simply by changing the direction ordering so as to change the occurrence of the -y move. In that case, the direction order routing method could be chosen as (+x, -y, z, -x, +y, -z) and the packet to be transferred between node 12.7 and node 12.11 will be transferred from node 12.7 to node 12.8 and then through nodes 12.5 and 12.2 to node 12.11, col: 5, lines: 63-67).

Consider **Claim:** 21, and as applied to Claim: 8 above, Thorson as modified by Passint discloses the method according to claim 8. Further taught by combination and specifically by Passint, wherein each switching element or a plurality of switching elements is mounted on a switching board (router pc board includes multiple routers,

col: 9, lines: 17-18), and the switching board is mounted on a unit cell through a socket, and wherein the unit cell is defined by n-tuple frames which are arranged in corresponding dimension, a wiring is formed along the frames to the socket (col: 9, lines: 17-18).

Consider **Claim:** 23, and as applied to Claim: 9 above, Thorson as modified by Passint discloses the method according to claim 9. Further taught by combination and specifically by Passint, wherein each switching element or a plurality of switching elements is mounted on a switching board (PC board 86 includes four routers, col: 9, lines: 23-24), and the switching board is mounted on a unit cell through a socket, and wherein the unit cell is defined by n-tuple frames which are arranged in corresponding dimension, a wiring is formed along the frames to the socket (Each of the four routers 50 on router PC board 86 is coupled to two nodes which are labeled N. Each node in the embodiment illustrated in FIG. 10 comprises two processors labeled P, col: 9, lines: 23-33).

Consider **Claim:** 24, and as applied to Claim: 10 above, Thorson as modified by Passint discloses the method according to claim 10. Further taught by combination and specifically by Passint, wherein each switching element or a plurality of switching elements is mounted on a switching board (PC board 86 includes four routers, col: 9, lines: 23-24), and the switching board is mounted on a unit cell through a socket, and wherein the unit cell is defined by n-tuple frames which are arranged in corresponding dimension, a wiring is formed along the frames to the socket (Each of the four routers 50 on router PC board 86 is coupled to two nodes which are labeled N. Each node in

the embodiment illustrated in FIG. 10 comprises two processors labeled P, col: 9, lines: 23-33).

Consider **Claim:** 25, Thorson discloses a switching system comprising: n-dimensionally arranged frames; n-dimensional unit cells defined by n-tuple frames of each dimension (Fig: 1); wherein a protocol processing block is connected to the switching boards mounted in unit cells located at outer surface or located interior remote from the outer surface are connected to a input output protocol processing block (In order to transfer a packet info from a source node to a destination node within the network, routing information is formed and transformed, col: 8, lines: 4-7; additionally fig: 5 @ 52 processor; and Each look-up table entry 62 includes dimension locations 66.1-66.3 and sign bits 68.1-68.3 for each of the n possible dimensions. (As was explained earlier, the sign bits indicate whether movement is to be in the PLUS or MINUS direction in a dimension), col: 10, lines: 44-48), and an outer traffic link is connected to the input output processing block (fig: 5 @ 52 processor). Even though, Thorson discloses processing block and switching boards, is generally silent about switching boards mounted in unit cell. However in the same field of endeavor, Passint et al. discloses that switching boards mounted in unit cell (Router pc board 86 includes four routers).

Therefore it would have been obvious to a person with ordinary skill in the art at the time the invention was made to incorporate and establishing a method for routing a packet between a source and a destination node in a network system with n-

dimensional topology as disclosed by Thorson with the method of Passint for increased fault tolerance.

Consider **Claim:** 26, and as applied to Claim: 25 above, Thorson as modified by Passint discloses the method according to claim 25. Further taught by combination and specifically by Passint, wherein some of the unit cells does not have the switching board (Fig: 10, 1 and 3).

Claims 22, and 27 are rejected under 35 U.S.C. 103 (a) as being unpatentable over **Thorson (US 5533198)** in view of **Passint et al. (US 6230252 B1)**, and further in view of **Brock et al. (6836849 B2).**

Consider **Claim:** 22, and as applied to Claim: 21 above, Thorson as modified by Passint discloses the method according to claim 21. However Thorson as modified by Passint is generally silent about coolant is flow inside the frame or the frame is in contact with a low temperature object. In the same field of endeavor, Brock et al. discloses coolant is flow inside the frame or the frame is in contact with a low temperature object (Fig: 3 cooling fan 322, and solid state cooling device 323). Therefore it would have been obvious to a person with ordinary skill in the art at the time the invention was made to incorporate and establishing a method for routing a packet between a source and a destination node in a network system with n-dimensional topology as disclosed by Thorson with the method of Passint for increased fault tolerance with the method disclosed by Brock for providing cooling fans for multiple and/or standalone processing units.

Consider **Claim:** 27, and as applied to Claim: 25 above, Thorson as modified by Passint discloses the method according to claim 25. However Thorson as modified by Passint is generally silent about each unit cells has a guide means on a surface or a corner of the frame for guiding an exchange apparatus for exchanging switching board. In the same field of endeavor, Brock et al. discloses, each unit cells has a guide means on a surface or a corner of the frame for guiding an exchange apparatus for exchanging switching board (Fig: 3, MS 304 inserted in the slot of the rack 301).

Conclusion

The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

- Nugent (U.S. Pub/Patent # 5175733) disclose: Adaptive message routing for multi-dimensional network.
- Wills (U.S. Pub/Patent # 5038398) disclose: Assigning communication links in a dynamic communication network
- Posner et al. (U.S. Pub/Patent # 4807280) disclose: Cross-Connect Switch.
- Morozov et al. (U.S. Pub/Patent # 5798580) disclose: Contention free global interconnection.
- Hills et al. (U.S. Pub/Patent # 4598400) disclose: Routing message packets
- Westfall et al. (U.S. Pub/Patent # 2005/0044195) disclose: Nodes interconnected by extended diagonal links.
- Hajikano et al. (U.S. Pub/Patent # 4837855) disclose: Non-blocking optical space switch.

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents

P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ketan Soni whose telephone number is (571) 270-1782. The Examiner can normally be reached on Monday-Thursday from 7:30am to 6:00pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Vu, Huy D. can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 703-305-3028. If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

Ketan Soni

ks

Nov 20, 2007.

HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600